Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A circuit arrangement for controlling a display device which can be operated in a partial mode, the circuit arrangement comprising:

a row drive circuit for driving n rows of the display device sequentially from 1 to n, the row drive circuit responsive to a row enable signal that is provided to each row from 1 to n; and

a column drive circuit for driving m columns of the display device by supplying column voltages to the m columns, the column voltages corresponding to picture data to be displayed as pixels of the controlled row, characterized in that a logic function is included in the row drive circuit in front of ~~at least one~~ row outputs, the logic function configured and arranged to respond to a first control signal~~,~~ having one or more pulses indicative of whether or not the partial mode is to be implemented, by preventing one or more of the ~~at least one~~ row outputs from driving one or more of the rows in response to the row enable signal;

wherein the row drive circuit comprises a shift register which has n stages and n outputs, and in that a second control signal can be supplied to the shift register at an input thereof for controlling the consecutive rows 1 to n, which second control signal activates the outputs of the shift register consecutively in dependence on pulses of a clock signal, and wherein the logic function is connected between the n outputs of the shift register and the n rows of the display, the logic function configured to prevent the n outputs of the shift register from driving any of the n rows of the display responsive to and during the one or more pulses of the first control signal;

wherein a frequency of the pulses of the clock signal increases during the one or more pulses of the first control signal.

2. (Previously presented) A circuit arrangement as claimed in claim 1, characterized in that the logic function is connected in front of each row output.

3. (Previously presented) A circuit arrangement as claimed in claim 1, characterized in that the logic function is realized as an AND gate.

Claim 4: Cancelled.

5. (Previously presented) A circuit arrangement as claimed in claim 2, characterized in that the first control signal is capable of switching off all n row outputs by means of the logic function during control of a line that is not to be displayed in the partial mode.

6. (Previously presented) A circuit arrangement as claimed in claim 1, characterized in that control logic in the column drive circuit generates the first control signal in dependence on the partial mode and supplies the first control signal to the row drive circuit.

7. (Previously presented) A circuit arrangement as claimed in claim 1, characterized in that the column drive circuit supplies no column voltages to the m columns in a case of a line that is not to be displayed.

Claim 8: Cancelled.

9. (Currently Amended) A row drive circuit for controlling n rows of a display device that is operable in a partial mode, the row drive circuit comprising:

a shift register having n stages and n outputs; and

a logic function connected in front of each of the n outputs of the shift register, the logic function configured to deactivate the n outputs of the shift register in dependence on the partial mode responsive to and during one or more pulses of a first control signal by preventing the n outputs of the shift register from driving the n rows of the display device;

wherein the outputs of the shift register are activated consecutively in dependence on pulses of a clock signal, and wherein a frequency of the pulses of the clock signal increases during the one or more pulses of the first control signal.

10. (Previously presented) A display device comprising a circuit arrangement as claimed in claim 1.

11. (Previously presented) An electronic appliance comprising a display device as claimed in claim 10.

12. (Currently Amended) A method of realizing a partial mode of a display device, the display device controlled by a circuit arrangement that includes a row drive circuit for driving n rows and a column drive circuit for supplying column voltages to m columns, the method comprising:

sequentially providing an enable signal to each row from 1 to n in response to pulses of a clock signal;

supplying the column voltages to the m columns for displaying corresponding picture data,

deactivating all row outputs of a first row of the row drive circuit, in response to a pulse of a first control signal indicating that a first plurality of rows are ~~the first row is~~ not to be displayed in the partial mode of the display device, by preventing the row outputs of the first plurality of rows from driving the display device during the pulse of the first control signal, and

activating all row outputs of one or more ~~a second~~ rows subsequent to the first plurality of rows~~,~~ in response to the enable signal and the end of the first control signal pulse indicating that the one or more rows are ~~second row is~~ to be displayed in the partial mode;

wherein a frequency of the pulses of the clock signal increases during the pulse of the first control signal.

13. (Previously presented) A circuit arrangement as claimed in claim 4, wherein each of the stages includes a flipflop.

14. (Previously presented) A circuit arrangement as claimed in claim 4, wherein the first control signal overrides the second control signal.